WHAT IS CLAIMED IS:

1. Control circuitry for adjusting a power supply level, VDD, of a digital processing component having varying operating frequencies, said control circuitry comprising:

N delay cells coupled in series, each of said N delay cells having a delay D determined by a value of VDD, such that a clock edge applied to an input of a first delay cell ripples sequentially through said N delay cells; and

power supply adjustment circuitry capable of adjusting VDD, said power supply adjustment circuitry operable to (i) monitor outputs of at least a K delay cell and a K+1 delay cell, (ii) determine that said clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell, and (iii) generate a control signal capable of adjusting VDD.

2. The control circuitry for adjusting a power supply level as set forth in Claim 1 wherein said power supply adjustment circuitry determines that said clock edge has reached said K delay cell output and has not reached said K+1 delay cell output when a next sequential clock edge is applied to said first delay cell input.

3. The control circuitry for adjusting a power supply level as set forth in Claim 2 wherein a total delay from said first delay cell input to said K delay cell output is greater than a maximum delay of said digital processing component scaled by a constant factor.

4. The control circuitry for adjusting a power supply level as set forth in Claim 2 wherein said power supply adjustment circuitry increases VDD if said clock edge has not reached said K delay cell output.

5. The control circuitry for adjusting a power supply level as set forth in Claim 2 wherein said power supply adjustment circuitry decreases VDD if said clock edge has reached said K+1 delay cell output.

6. The control circuitry for adjusting a power supply level as set forth in Claim 2 wherein said power supply adjustment circuitry is further operable to monitor outputs of at least a K-1 delay cell, said K delay cell, said K+1 delay cell, and a K+2 delay cell.

7. The control circuitry for adjusting a power supply level as set forth in Claim 6 wherein said power supply adjustment circuitry is further operable to determine that said clock edge has reached an output of said K-1 delay cell and said K delay cell output and has not reached said K+1 delay cell output.

8. The control circuitry for adjusting a power supply level as set forth in Claim 7 wherein said power supply adjustment circuitry increases VDD in relatively large incremental steps if said clock edge has not reached said K-1 delay cell output.

9. The control circuitry for adjusting a power supply level as set forth in Claim 8 wherein said power supply adjustment circuitry increases VDD in relatively small incremental steps if said clock edge has reached said K-1 delay cell output but has not reached said K delay cell output.

10. The control circuitry for adjusting a power supply level as set forth in Claim 7 wherein said power supply adjustment circuitry decreases VDD in relatively large incremental steps if said clock edge has reached said K+1 delay cell output and said K+2 delay cell output.

11. The control circuitry for adjusting a power supply level as set forth in Claim 10 wherein said power supply adjustment circuitry decreases VDD in relatively small incremental steps if said clock edge has reached said K+1 delay cell output but has not reached said K+2 delay cell output.

12. A method of operating control circuitry for adjusting a power supply level, VDD, of a digital processing component having varying operating frequencies, said method of operating said control circuitry comprising the steps of:

applying a clock edge to an input of a first one of N delay cells coupled in series, each of said N delay cells having a delay D determined by a value of VDD, said applied clock edge rippling sequentially through said N delay cells;

monitoring outputs of at least a K delay cell and a K+1 delay cell;

determining that said clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell; and

generating a control signal capable of adjusting VDD.

13. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 12 further comprising the step of determining that said clock edge has reached said K delay cell output and has not reached said K+1 delay cell output when a next sequential clock edge is applied to said first delay cell input.

14. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 13 wherein a total delay from said first delay cell input to said K delay cell output is greater than a maximum delay of said digital processing component scaled by a constant factor.

15. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 13 further comprising the step of increasing VDD if said clock edge has not reached said K delay cell output.

16. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 13 further comprising the step of decreasing VDD if said clock edge has reached said K+1 delay cell output.

17. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 13 further comprising the step of monitoring outputs of at least a K-1 delay cell, said K delay cell, said K+1 delay cell, and a K+2 delay cell.

18. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 17 further comprising the step of determining that said clock edge has reached an output of said K-1 delay cell and said K delay cell output and has not reached said K+1 delay cell output.

19. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 18 further comprising the step of increasing VDD in relatively large incremental steps if said clock edge has not reached said K-1 delay cell output.

20. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 19 further comprising the step of increasing VDD in relatively small incremental steps if said clock edge has reached said K-1 delay cell output but has not reached said K delay cell output.

21. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 18 further comprising the step of decreasing VDD in relatively large incremental steps if said clock edge has reached said K+1 delay cell output and said K+2 delay cell output.

22. The method of operating control circuitry for adjusting a power supply level, VDD, as set forth in Claim 21 further comprising the step of decreasing VDD in relatively small incremental steps if said clock edge has reached said K+1 delay cell output but has not reached said K+2 delay cell output.

23. A digital circuit comprising:

a digital processing component capable of operating at different clock frequencies;

an adjustable clock source capable of supplying variable clock frequencies to said digital processing component;

an adjustable power supply capable of supplying a variable power supply level, VDD, to said digital processing component; and

control circuitry for adjusting VDD comprising:

N delay cells coupled in series, each of said N delay cells having a delay D determined by a value of VDD, such that a clock edge applied to an input of a first delay cell ripples sequentially through said N delay cells; and

power supply adjustment circuitry capable of adjusting VDD, said power supply adjustment circuitry operable to (i) monitor outputs of at least a K delay cell and a K+1 delay cell, (ii) determine that said clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell, and (iii) generate a control signal capable of adjusting VDD.

24. The digital circuit as set forth in Claim 23 wherein said power supply adjustment circuitry determines that said clock edge has reached said K delay cell output and has not reached said K+1 delay cell output when a next sequential clock edge is applied to said first delay cell input.

25. The digital circuit as set forth in Claim 24 wherein a total delay from said first delay cell input to said K delay cell output is greater than a maximum delay of said digital processing component.

26. The digital circuit as set forth in Claim 24 wherein said power supply adjustment circuitry increases VDD if said clock edge has not reached said K delay cell output.

27. The digital circuit as set forth in Claim 24 wherein said power supply adjustment circuitry decreases VDD if said clock edge has reached said K+1 delay cell output.

28. The digital circuit as set forth in Claim 24 wherein said power supply adjustment circuitry is further operable to monitor outputs of at least a K-1 delay cell, said K delay cell, said K+1 delay cell, and a K+2 delay cell.

29. The digital circuit as set forth in Claim 28 wherein said power supply adjustment circuitry is further operable to determine that said clock edge has reached an output of said K-1 delay cell and said K delay cell output and has not reached said K+1 delay cell output.

30. The digital circuit as set forth in Claim 29 wherein said power supply adjustment circuitry increases VDD in relatively large incremental steps if said clock edge has not reached said K-1 delay cell output.

31. The digital circuit as set forth in Claim 30 wherein said power supply adjustment circuitry increases VDD in relatively small incremental steps if said clock edge has reached said K-1 delay cell output but has not reached said K delay cell output.

32. The digital circuit as set forth in Claim 29 wherein said power supply adjustment circuitry decreases VDD in relatively large incremental steps if said clock edge has reached said K+1 delay cell output and said K+2 delay cell output.

33. The digital circuit as set forth in Claim 32 wherein said power supply adjustment circuitry decreases VDD in relatively small incremental steps if said clock edge has reached said K+1 delay cell output but has not reached said K+2 delay cell output.